Listing of Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1 - 7 (canceled)

8. (Currently amended) A method of manufacturing a semiconductor integrated circuit device, comprising:

forming a first transistor of a MIS depletion type and a second transistor forming part of a masked ROM on a single semiconductor substrate by:

forming a well region of a first-conductivity-type in a first region where the first transistor is to be formed and a second region where the second transistor is to be formed;

implanting impurity ions of a first-conductivity-type in the regions where the first and second transistors are to be formed to form a channel region;

implanting impurity ions of a second-conductivity-type in the channel regions ~~where~~ of the first and second transistors ~~are to be formed~~ to permit current to flow when a gate-source voltage of the first transistor is zero and to change the second transistor into resistance, said implanting of impurity ion of said second conductivity type in both of said channel regions being carried out in the same ion implantation step; and thereafter

forming a gate insulating film, a gate electrode, and source and drain regions of a second-conductivity-type in each of the first and second transistors.

9. (Previously added) A method of manufacturing a semiconductor integrated circuit device, as claimed in claim 8, further comprising:

selectively forming a field oxide on the well region, wherein the field oxide separates the regions in which the first and second transistors are formed.

10. (New) A method of manufacturing a semiconductor integrated circuit device, as claimed in claim 8, additionally comprising forming a first LDD region of a second-conductivity-type having a lower impurity concentration than the first source region or the first drain region, formed between the first channel region and the first source region and between the first channel region and the first drain region.

11. (New) A method of manufacturing a semiconductor integrated circuit device, as claimed in claim 10, additionally comprising forming a second LDD region of a second-conductivity-type having a lower impurity concentration than the second source region or the second drain region, formed between the second channel region and the second source region and between the second channel region and the second drain region.

12. (New) A method of manufacturing a semiconductor integrated circuit device, as claimed in claim 8, additionally comprising forming a punch-through stopper region of a first-conductivity-type formed between the first source region and the first drain region and between the second source region and the second drain region.

13. (New) A method of manufacturing a semiconductor integrated circuit device, as claimed in claim 12, additionally comprising forming an enhancement type NMOS transistor and an enhancement type PMOS transistor on said single semiconductor substrate.

14. (New) A method of manufacturing a semiconductor integrated circuit device, as claimed in claim 13, wherein said NMOS transistor is formed in a P-type well region, and includes a third source region of an N-type and a third drain region an N-type formed in the P-type well region, and a third channel region interposed between the third source and drain regions, a third LDD region of an N-type having a lower impurity concentration than the third source region or the third drain region formed between the third channel region and the third source region and between the third channel region and the third drain region, a third gate electrode formed on the third channel region over the gate insulating film, and a P-type punch-through stopper region formed between the third source region and the third drain region.

15. (New) A method of manufacturing a semiconductor integrated circuit device, as claimed in claim 13, wherein said PMOS transistor is formed in an N-type well region, and comprises a fourth source region of a P-type and a fourth drain region of a P-type formed in the N-type well region, a fourth channel region interposed between the fourth source and drain regions, and a fourth LDD region of a P-type having a lower impurity concentration than the fourth source region or the fourth drain region formed between the fourth channel region and the fourth source region and between the fourth channel region and the fourth drain region, a fourth gate electrode formed on the fourth channel region over the gate insulating film, and an N-type punch-through stopper region formed between the fourth source region and the fourth drain region.

16. (New) A method of manufacturing a semiconductor integrated circuit device, as claimed in claim 8, further comprising forming a first-conductivity-type punch-through stopper region provided between the first source region and the first drain region.

17. (New) A method of manufacturing a semiconductor integrated circuit device, as claimed in claim 8, further comprising forming a first conductivity-type punch-through stopper region between the second source region and the second drain region.

18. (New) A method of manufacturing a semiconductor integrated circuit device, as claimed in claim 8, wherein said first conductivity type is P-type and said second conductivity type is N-type.

19. (New) A method of manufacturing a semiconductor integrated circuit device, as claimed in claim 8, wherein said first conductivity type is N-type and said second conductivity type is P-type.